AF/ZIW

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.	:	09/611,037
Applicant:	:	Kuthi, et al.
Filed:	:	July 6, 2000
Title:	:	METHOD FOR IMPLEMENTING A SEMICONDUCTOR PROCESS CHAMBER ELECTRODE
TC/A.U.	:	1763
Examiner	:	Alejandro Mulero, L.
Atty. Docket No.	:	LAM1P077A
Date:	:	September 13, 2005

CERTIFICATE OF MAILING
I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on **September 13, 2005**.

Signed: Lauren Leschauer
Lauren Leschauer

REINSTATEMENT OF APPEAL AND TRANSMITTAL OF SUPPLEMENTAL APPEAL BRIEF

Commissioner for Patents
Mail Stop: Appeal Brief- Patents
Alexandria, VA 22313-1450

Sir:

Applicants hereby reinstate the Appeal in this matter. The Notice of Appeal was filed on November 29, 2004, and an Appeal Brief was filed on March 3, 2005. Following Applicants' Appeal Brief, a non-final action was mailed on May 13, 2005. The period for response expired on August 13, 2005. Applicants hereby petition for a one-month extension of the period in which to reply, extending the period for response to September 13, 2005.

Applicants assert and/or enclose the following:

The Notice of Appeal fee has already been paid.

The fee for filing the Appeal Brief has already been paid.

Applicants herewith enclose a Supplemental Appeal Brief.

09/16/2005 TBESHAH1 00000015 09611037
01 FC:1251 120.00 OP

Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

Months	Large Entity	Small Entity
☒ one	$120.00	$60.00
☐ two	$450.00	$225.00
☐ three	$1,020.00	$510.00

If an additional extension of time is required, please consider this a petition therefor.

Total Fees Due:

Notice of Appeal Fee	$ 0
Extension Fee (if any)	$120.00
Total Fee Due	**$120.00**

Enclosed is Check No. 14919 in the amount of $120.00.

Charge any additional fees or credit any overpayment to Deposit Account No. 50-0850, (Order No. LAM1P077A).

Respectfully submitted,
MARTINE PENILLA & GENCARELLA, LLP

Rick von Wohld, Esq.
Registration No. 48,018

710 Lakeway Drive, Suite 200
Sunnyvale, CA 94085
(408) 749-6900
Customer No. 25920

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

EX PARTE KUTHI, ET AL.

Application for Patent

Filed July 6, 2000

Application No. 09/611,037

FOR:

METHOD FOR IMPLEMENTING A SEMICONDUCTOR PROCESS CHAMBER ELECTRODE

SUPPLEMENTAL APPEAL BRIEF

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Signed: Lauren Leschauer
Lauren Leschauer

MARTINE PENILLA & GENCARELLA, LLP
Attorneys for Applicants

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I. REAL PARTY IN INTEREST

The real party in interest is Lam Research Corporation, the assignee of the present application.

II. RELATED APPEALS AND INTERFERENCES

The present application is a parent application of continuation application, U.S. Patent Application Serial No. 10/796,836. A Notice of Appeal was filed for 10/796,836 on June 17, 2005, and an Appeal Brief was filed on August 22, 2005.

III. STATUS OF THE CLAIMS

A total of 40 claims were presented during the prosecution of the present application. Applicants canceled claims 1-13 and 22-32. Applicant appeals the final rejection of claims 14-21 and 33-40.

IV. STATUS OF THE AMENDMENTS

No Amendment has been filed subsequent to Final Rejection.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

In one embodiment of the invention, Applicants claim a method for processing a semiconductor wafer through plasma etching operations. The method is claimed in a chamber for processing a semiconductor wafer through plasma etching operations, the chamber being in an operational state and including a support chuck for holding the semiconductor wafer, a pair of RF power sources, and a top electrode (see Applicants' specification as filed, page 6, lines 8-12, Figure 1A). The method includes striking a plasma in a plasma region of the chamber, and generating an increase in bias voltage directed at a wafer surface of the semiconductor wafer, and a decrease in bias voltage directed at the top electrode (page 16, line 19 - page 17, line 7, Figure 4A). The top electrode includes a center region, a first surface and a second surface. The first surface includes an inlet that is configured to receive processing gases from a source that is external to the chamber, and to flow the processing gases into the center region. The second surface includes a plurality of gas feed holes (228, Figs. 2A, 2E) that lead to a plurality of electrode openings (202b, Figs. 2A, 2B, 2C, 2D, 2E) that have electrode opening diameters (242, Figs. 2C, 2D) that are greater than gas feed hole diameters (240, Figs. 2C, 2D) of the plurality of gas feed holes

(228). The plurality of electrode openings (202b) are configured to define the second surface which is located over the wafer surface (236, Fig. 2E) of the semiconductor wafer. According to the method, when a plasma is struck in the plasma region (212, Fig. 2E) defined between the second surface and the wafer surface, the plasma defines a first plasma sheath surface (232, Fig. 2E) having a first plasma sheath surface area that is proximate to the wafer surface, and a second plasma sheath surface (231, Fig. 2E) having a second plasma sheath surface area that is proximate to the second surface. The second plasma sheath surface area is greater than the first plasma sheath surface area (Figs. 2E, 3, and page 14, line 11 - page 15, line 6, Table A).

In another embodiment, Applicants claim a method of processing a semiconductor wafer. The method includes providing a processing chamber. The processing chamber is in an operational state and includes a top electrode, a wafer support chuck having the semiconductor wafer positioned thereon, and a pair of RF power sources (see Applicants' specification as filed, page 6, lines 8-12, page 13, lines 19-22, Figure 1A). The method further includes striking a plasma within a plasma region (212, Fig. 2E) of the processing chamber, and causing a first surface of a plasma sheath (231, Fig. 2E) to shift (Figs. 2E, 3, 4A) into electrode openings (202b, Figs. 2A, 2B, 2C, 2D, 2E) of the top electrode. The plasma sheath defines the first surface of the plasma sheath (231, Fig. 2E) next to the top electrode (200, Fig. 2A) and a second surface (232, Fig. 2E) of the plasma sheath over a surface of the semiconductor wafer (206, Fig. 2E).

In a further embodiment, Applicants claim a method for high aspect ratio semiconductor etching (page 17, lines 16-21). The method includes providing a plasma etch processing chamber. The plasma etch processing chamber includes a top electrode, a wafer support chuck, and a pair of RF power supplies (see Applicants' specification as filed, page 6, lines 8-12, Figure 1A). The plasma etch processing chamber is configured to be in an operational state (page 13, lines 19-22). The method further includes striking a plasma in a plasma region (212, Fig. 2E) of the plasma etch processing chamber. The plasma region is defined between an electrode surface of the top electrode (200, Fig. 2A), and a wafer surface of a wafer positioned on the wafer support chuck (206, 236, Fig. 2E). The method then includes causing a first surface (231 Figs. 2E, 3) of a plasma sheath to shift into electrode openings of the

top electrode (202b, Fig. 2E). The first surface of the plasma sheath is proximate to the top electrode. The method provides for increasing a bias voltage over the wafer surface while decreasing the bias voltage over the electrode surface of the top electrode without increasing a plasma density (Page 17, lines 1-23, Figs. 4A, 4B, 5).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The grounds for rejection to reviewed on appeal are as follows:

Claims 33-35, 37-38, and 40 were rejected under 35 USC §103(a); and

Claims 14-21, and 33-40 were rejected under 35 USC §103(a).

VII. ARGUMENT

An Appeal Brief was filed in the present application following a Notice of Appeal filed on November 29, 2004 in response to a Final action of September 2, 2004. In response to Applicants' Appeal Brief of March 3, 2005, the Office replied with a non-final action, which re-opened prosecution by implication. Applicants acknowledge that the previously asserted 35 USC §112, second paragraph, rejections have been dropped, the asserted "new grounds" for the remaining rejections are essentially similar to the previously asserted rejections. Applicants therefore reinstate the Appeal in this matter, file the instant Supplemental Appeal Brief to address the "new grounds" for rejection, and hereby incorporate by reference the Appeal Brief filed on March 3, 2005.

A. Claims 33-35, 37-38, and 40 are not rendered obvious by the patent to Tomita et al. in view of admitted prior art.

Claims 33-35, 37-38, and 40 stand rejected under 35 USC §103(a) as being unpatentable over Tomita et al. (U.S. Patent No. 5,593,540) in view of admitted prior art.

Tomita et al. disclose a plasma etching system including a process chamber for enclosing a plasma, and a means for evacuation of the plasma from the chamber. A substrate is supported on a chuck electrode, and a shower electrode is positioned facing the chuck electrode. The shower electrode has a plurality of small holes. A power source is provided to strike a plasma between the chuck electrode and the shower electrode. Plasma forming gases are supplied through the small holes into the

space between the chuck electrode and the shower electrode. The gas is supplied through the small holes at a mass flow rate of at least 620 kg/m^2/hr.

Applicants' independent claim 33 claims a method of processing a semiconductor wafer. The method includes providing a processing chamber. The processing chamber is in an operational state and includes a top electrode, a wafer support chuck that has the semiconductor wafer positioned thereon, and a pair of RF power sources. The method then includes striking a plasma within a plasma region of the processing chamber, and causing a first surface of a plasma sheath to shift into electrode openings of the top electrode. The plasma sheath defines the first surface of the plasma sheath next to the top electrode and a second surface of the plasma sheath over a surface of the semiconductor wafer.

Applicants' independent claim 37 claims a method for high aspect ratio semiconductor etching. The method includes providing a plasma etch processing chamber which includes a top electrode, a wafer support chuck, and a pair of RF power supplies, and is configured in an operational state. A plasma is struck in a plasma region of the chamber. The plasma region is defined between an electrode surface of the top electrode and a wafer surface of a wafer which is positioned on the wafer support chuck. A first surface of a plasma sheath which is proximate to the top electrode is caused to shift into electrode openings of the top electrode. A bias voltage over the wafer surface is increased while the bias voltage over the electrode surface of the top electrode is decreased without increasing a plasma density.

In rejecting claims 33-35, 37-38, and 40, the Examiner maintains the assertion of the Tomita et al. reference teaching all of the structural elements of Applicants' method claims, and that the method operations of causing the first surface of the plasma sheath to shift into the electrode openings of the top electrode and forming a plasma sheath having a first surface and a second surface is just inherent in the structure of Tomita et al.

Applicants submit that 1) the structure of Tomita et al. does not inherently cause a shift of the plasma sheath into electrode openings, and 2) the electrode size parameter of the Tomita et al. reference does not teach or suggest the method that Applicants claim.

Regarding 1) the structure of the Tomita et al. apparatus, Applicants have repeatedly addressed the failure of the Office's inherency assertion. Applicants therefore respectfully direct the Board to the inherency argument of record, and in

Applicants' Appeal Brief of March 3, 2005, which has been incorporated herein by reference.

Regarding 2) the electrode size parameter of the Tomita et al. reference does not teach or suggest the method Applicants claim, the asserted "teaching" is both antithetical to the reference invention, and does not support a *prima facie* case of obviousness.

Tomita et al. teaches in structure, processing parameters, and invention objective to prevent or suppress polymerization within gas feed holes of the showerhead. The reference teaches gas flow rate, chamber pressure, cathode plate temperature and other process parameters in order to maintain sufficient mass flow and plasma processing within the chamber for anisotropic etching with a high aspect ratio. The reference does not teach the formation of a plasma sheath, does not teach the properties of a plasma sheath, does not teach surfaces of a plasma sheath, and most certainly does not teach formation of a first surface area of a first surface of the plasma sheath that is larger than a second surface area of a second surface of the plasma sheath by shifting the first surface of the plasma sheath into the electrode openings.

Tomita et al. does discuss polymerization that is deposited on or forms in the gas feed holes. The reference *does not* teach or suggest the real effect that such deposits or formation has on the plasma sheath. The reference does discuss a particular type of etching operation, *i.e.*, an anisotropic etching operation, but the reference neither teaches nor suggests the formation of the plasma sheath and associated surfaces, and the effects of manipulation of the plasma sheath surfaces and associated surface areas on ion bombardment energy. Applicants have specifically claimed shifting the first surface of the plasma sheath into the electrode openings of the top electrode. And, the term "shifting" is and must be read in light of Applicants' disclosure, which makes clear that it is not simply "incidental" (see page 17, and Figures 3-5). The combination of Tomita et al. and admitted prior art simply does not teach or suggest all the claim elements of Applicants' independent claims 33 and 37, and therefore likewise does not teach or suggest the claim elements of Applicants claims 33-35, 37-38, and 40. Applicants therefore submit that these rejections are improper and should be withdrawn.

B. Claims 14-21, and 33-40 are not rendered obvious by admitted prior art in view of the patent to Chang et al., or alternatively, by the patent to Chang et al. in view of admitted prior art.

Claims 14-21, 33-40 stand rejected under 35 USC §103(a) as being unpatentable over 1) admitted prior art in view of Chang et al. (U.S. Patent No. 4,854,263), and 2) Chang et al. in view of admitted prior art.

Similar to the rejections addressed above in section "A," the Office has cited the structure of the apparatus described by Chang et al., and asserted that it teaches the method claimed by Applicants. As stated previously, the size of the gas feed holes, or electrode openings, is but one parameter of many parameters in one of a plurality of etch processes. The Office has done little more than assert that, because the dimension of the gas feed holes of Chang et al. are within the range of the dimension of Applicants' electrode openings, the reference, in combination with prior art, teaches the claimed method. The asserted combination, however, does not speak to Applicants' currently claimed method. The asserted combination does not teach, disclose, suggest, describe, aver, or otherwise hint at the formation of a plasma having a plasma sheath, that the plasma sheath has a first surface having a first surface area and a second surface having a second surface area and that the first surface is shifted into the electrode openings so that the first surface area is greater than the second surface area which increases the ion bombardment directed at the wafer surface which is particularly effective in high aspect ratio etching. The asserted combination neither teaches nor suggests the claimed method, and the Office has done little more than proclaim that a structural similarity which is but one parameter of a plurality of parameters in an etch process renders the claimed method obvious. Such a proclamation fails to support a *prima facie* case of obviousness.

Applicants therefore submit that the rejection of claims 14-21, and 33-40 under 35 USC §103(a) as being unpatentable over 1) admitted prior art in view of Chang et al., and 2) Chang et al. in view of admitted prior art is improper and should be withdrawn.

Respectfully submitted,
MARTINE PENILLA & GENCARELLA, LLP

Rick von Wohld, Esq.
Reg. No. 48,018

MARTINE PENILLA & GENCARELLA, LLP
710 Lakeway Drive, Suite 200
Sunnyvale, California 94085
Customer Number 25920

APPENDIX A

CLAIMS ON APPEAL

14. In a chamber for processing a semiconductor wafer through plasma etching operations, the chamber being in an operational state and including a support chuck for holding the semiconductor wafer, a pair of RF power sources, and a top electrode, a method for processing a semiconductor wafer through plasma etching operations, comprising:

striking a plasma in a plasma region of the chamber; and

generating an increase in bias voltage directed at a wafer surface of the semiconductor wafer and a decrease in bias voltage directed at the top electrode, the top electrode having a center region, a first surface and a second surface, the first surface having an inlet that is configured to receive processing gases from a source that is external to the chamber and flow the processing gases into the center region, the second surface having a plurality of gas feed holes that lead to a plurality of electrode openings that have electrode opening diameters that are greater than gas feed hole diameters of the plurality of gas feed holes, the plurality of electrode openings being configured to define the second surface which is located over the wafer surface of the semiconductor wafer,

wherein when a plasma is struck in the plasma region defined between the second surface and the wafer surface, the plasma defines a first plasma sheath surface having a first plasma sheath surface area that is proximate to the wafer surface and a second plasma sheath surface having a second plasma sheath surface area that is proximate to the second surface, the second plasma sheath surface area being greater than the first plasma sheath surface area.

15. The method for processing a semiconductor wafer through plasma etching operations as recited in claim 14, further comprising:

coupling the top electrode to one of the pair of RF power sources and the support chuck to the other one of the pair of RF power sources.

16. The method for processing a semiconductor wafer through plasma etching operations as recited in claim 14, further comprising:

causing the second plasma sheath surface having the second plasma sheath surface area to shift into the electrode openings of the second surface of the top electrode, the electrode openings being at least 0.5 mm or greater in diameter and the gas feed holes having a diameter of about 0.1 mm.

17. The method for processing a semiconductor wafer through plasma etching operations as recited in claim 16, further comprising:

defining the electrode openings to a depth of between about 1/32 inch and ¼ inch.

18. The method for processing a semiconductor wafer through plasma etching operations as recited in claim 16, further comprising:

fixing a separation of between about 0.75 cm and about 4 cm between the second surface and the wafer surface.

19. The method for processing a semiconductor wafer through plasma etching operations as recited in claim 18, further comprising:

inserting two or more gas buffer plates within the center region of the top electrode.

20. The method for processing a semiconductor wafer through plasma etching operations as recited in claim 18, further comprising:

fixing a separation between the second plasma sheath surface having the second plasma sheath surface area and the second surface of the top electrode at between about 0.5 mm and about 5 mm.

21. The method for processing a semiconductor wafer through plasma etching operations as recited in claim 14, further comprising:

increasing an ion bombardment energy over the wafer surface when the second plasma sheath surface area is greater than the first plasma sheath surface area.

33. A method of processing a semiconductor wafer, comprising:

providing a processing chamber, the processing chamber being in an operational state and including a top electrode, a wafer support chuck having the semiconductor wafer positioned thereon, and a pair of RF power sources;

striking a plasma within a plasma region of the processing chamber; and

causing a first surface of a plasma sheath to shift into electrode openings of the top electrode,

wherein the plasma sheath defines the first surface of the plasma sheath next to the top electrode and a second surface of the plasma sheath over a surface of the semiconductor wafer.

34. The method of processing a semiconductor wafer as recited in claim 33, wherein a surface area of the first surface of the plasma sheath is greater than a surface area of the second surface of the plasma sheath.

35. The method of processing a semiconductor wafer as recited in claim 33, further comprising increasing a bias voltage over the surface of the semiconductor wafer while slightly decreasing the bias voltage over a surface of the top electrode and without increasing a plasma density.

36. The method of processing a semiconductor wafer as recited in claim 33, wherein the top electrode has a center region, a first surface and a second surface, the first surface of the top electrode having an inlet that is configured to receive processing gases from a source that is external to the processing chamber and to flow the processing gases into the center region, the second surface of the top electrode having a plurality of gas feed holes that lead to a plurality of electrode openings that have electrode opening diameters that are greater than gas feed hole diameters of the plurality of gas feed holes, the plurality of electrode openings being configured to define the second surface of the top electrode which is located over the surface of the semiconductor wafer.

37. A method for high aspect ratio semiconductor etching, comprising:

providing a plasma etch processing chamber, the plasma etch processing chamber including a top electrode, a wafer support chuck, and a pair of RF power supplies, and the plasma etch processing chamber being configured in an operational state;

striking a plasma in a plasma region of the plasma etch processing chamber, the plasma region being defined between an electrode surface of the top electrode and a wafer surface of a wafer positioned on the wafer support chuck;

causing a first surface of a plasma sheath to shift into electrode openings of the top electrode, the first surface of the plasma sheath being proximate to the top electrode; and

increasing a bias voltage over the wafer surface while decreasing the bias voltage over the electrode surface of the top electrode and without increasing a plasma density.

38. The method for high aspect ratio semiconductor etching of claim 37, further comprising increasing an ion bombardment energy on the wafer surface.

39. The method for high aspect ratio semiconductor etching of claim 37, wherein the top electrode has a center region, a first surface and the electrode surface, the first surface of the top electrode having an inlet that is configured to receive processing gases from a source that is external to the processing chamber and to flow the processing gases into the center region, the electrode surface of the top electrode having a plurality of gas feed holes that lead to a plurality of electrode openings that have electrode opening diameters that are greater than gas feed hole diameters of the plurality of gas feed holes, the plurality of electrode openings being configured to define the electrode surface of the top electrode which is located over the wafer surface.

40. The method for high aspect ratio semiconductor etching of claim 37, wherein a surface area of the first surface of the plasma sheath is greater than a surface area of a second surface of the plasma sheath, the second surface of the plasma sheath being defined proximate to the wafer surface.

APPENDIX B

EVIDENCE APPENDIX

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.	:	09/611,037
Applicant:	:	Kuthi, et al.
Filed:	:	July 6, 2000
Title:	:	METHOD FOR IMPLEMENTING A SEMICONDUCTOR PROCESS CHAMBER ELECTRODE
TC/A.U.	:	1763
Examiner	:	Alejandro Mulero, L.
Atty. Docket No.	:	LAM1P077A

Declaration Under 37 CFR §1.132

I, Lumin Li, declare as follows:

1. I am a named inventor in the subject application. I earned an undergraduate degree in Electronic Engineering from Southeast University, and Ph.D. degree in Electrical Engineering from Colorado State University. I currently work in reactor design and process applications of plasma etcher, and have been employed for 11 years. For the past 8 years, I have been with Lam Research Corporation working on new dielectric etcher development.

2. I have reviewed the patent to Tomita et al. (U.S. Patent No. 5,593,540), the reference patent. The reference patent teaches how to prevent polymer deposition in the small holes of a showerhead electrode by high speed of gas flow. To achieve a mass flow speed of at least 620 $kg/m^2/hr$, the reference specifies the diameter of the holes in the showerhead must be smaller than 0.6 mm. The reference specifies 0.6 mm as the maximum diameter of the hole. Any hole larger than 0.6 mm will reduce gas speed and cannot prevent polymer deposition.

3. Our claimed invention described in the subject application is in the field of plasma physics. Our claimed invention teaches how to reduce sheath voltage next to the top electrode. By forming the plasma sheath inside the holes, the surface area of the plasma sheath next to the top electrode is increased, and its potential is reduced. The holes in the claimed invention must big enough to allow plasma to exist inside to form a hollow cathode discharge.

4. The diameter of the holes on the electrode showerhead is very critical for showerhead design. Increasing gas flow speed, and increasing the surface area of a plasma sheath are in different fields and have different technological focus. A large diameter of hole will reduce backside pressure, and will reduce gas flow speed through the holes. As a result, polymer may deposit inside holes. The reference patent specifies the maximum diameter of hole. Any hole larger than 0.6 mm will reduce gas speed and cannot prevent polymer deposition. On the contrary, hole size in our claimed invention must be bigger than a thickness of the plasma sheath to allow the sheath to form inside the hole. We specified the minimum hole size of 0.5 mm. The diameter of any hole larger than 0.5 mm will meet the requirement for a hole size, depending on various process parameters, including plasma sheath thickness.

5. Plasma sheath thickness depends on pressure, power and chemistry. For different etch applications, pressure in our etcher could vary from 10 mT to 2T, power could be 50W to 6KW, and there are more than 16 available gases. In order to include a wide range of plasma etch process regimes, we chose a diameter of 0.5 mm conservatively as the minimum size for the worst case with a high pressure, low power, and heavy polymer contents. For most of our applications, we prefer diameter of showerhead holes to be 2 ~ 10 mm.

6. Diameter of showerhead holes must be very small not only for gas flow speed, but also for preventing plasma light-up inside the hole. It is well known that when the hole is too large, and at high pressure, according to Paschen curve, plasma will ignite inside the hole. When plasma exists inside the hole, dense plasma inside of the hole will dissociate more species and generate more polymers inside the holes. As a result, there is or will be more polymer deposition. When plasma lights-up inside a hole, a sheath with high potential will accelerate ions and sputter away the electrode material. Plasma ignited inside a hole of showerhead is not desirable for a plasma etcher. The fast erosion of the electrode will quickly affect process repeatability, increase polymer deposition, and reduce lifetime of showerhead. It is a basic rule in plasma etcher design that the showerhead should prevent plasma light-up inside the hole. Our claimed invention purposely increases hole size and forms plasma in a portion of the hole, and is a

special case in which an increase in ion's energy on the wafer is critical for certain etch applications.

7. In our claimed invention, there are two different diameters of each hole specified for electrode showerhead design. The diameter of the hole in the top end and close to gas source (the gas feed holes) is 0.1 mm which is designed to prevent plasma from entering the holes and light-up inside of the holes and on a backside of the shower head. The diameter of the holes in the lower end and in contact with plasma (the electrode openings) is 0.5 mm which is designed to create plasma inside hole, increase the surface area of the plasma sheath next to the top electrode and increase the potential at the opposite electrode.

8. The objective of the reference patent is preventing polymer deposition. The size of the holes in the showerhead must be small enough to obtain the certain disclosed flow speed. At the same time, the flow speed must be maintained to prevent plasma light up inside the holes. A diameter of 0.6mm does not inherently shift the plasma sheath into the openings and create a surface area next to the electrode that is larger than the surface area that is next to the wafer. It is against common sense, basic plasma physics, and design rules for those skilled in the art -- that is, one of average competence and expertise in the field of plasma etch, would not modify the reference in such a manner as to increase size of the holes and purposely create plasma inside holes.

9. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 USC §1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

LUMIN LI

9-3-03
DATE

APPENDIX C

RELATED PROCEEDINGS APPENDIX

NOT APPLICABLE